

REMARKS

The following remarks are being submitted as a full and complete response to the Office Action dated July 14, 2008 and the telephone interview with the Examiner conducted on September 4, 2008. Applicants thank the Examiner for taking the time to conduct the telephone interview.

In view of the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-24 and 29-31 are under consideration in this application. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Interview Summary

Applicants, through their representative, Jennifer Teng, compared Fig. 2 of the present invention with Fig. 2 of Stewart, and explained to the Examiner that Stewart only supplies a constant voltage to a power supply line D2 connected to a source/drain of the OLED 210 in the illuminated period, but not to a signal line D1 connected to the gate of the OLED 210 in the illuminated period, as in the present invention. The Examiner indicated that he will take the explanation into consideration when he receives a formal response, since the case is under final rejection.

Prior Art Rejections

Under 35 U.S.C. §103(a), the Examiner rejected: (1) Claims 1-4, 6-7, 9, 12-15, 17-18, 20, 23-24 and 29-31 as being unpatentable over US Publication No. 2003/0067424 to Akimoto et al. in view of newly cited US Patent No. 5,952,789 to Stewart et al.; (2) Claims 5, 8, 16 and 19 as being unpatentable over Akimoto '424 in view of Stewart '789, and further in view of US Patent No. 5,250,931 to Misawa et al.; (3) Claims 10 and 21 as being unpatentable over Akimoto '424 in view of Stewart '789, and further in view of US Patent No. 6,670,936 to Akimoto et al.; and (4) Claims 11 and 22 as being unpatentable over Akimoto '424 in view of Stewart '789, and further in view of US Patent No. 6,812,912 to Miyajima et al. These rejections have been carefully considered, but are most respectfully traversed.

The image display device of the present invention (for example, the embodiment depicted in Figs. 1-4), as now recited in claim 1, comprises: a display part 20 configured by a plurality of pixels 10 each having an electro-luminescent element 1 driven to illuminate according to a display signal voltage V_s ; a signal line 8 used to write said display signal voltage V_s in said pixel 10 (during a “writing period”, 1st half of a frame in Fig. 3 with the timing details shown in Fig. 4); a pixel selector 15 for selecting a pixel from said plurality of pixels so as to write said display signal voltage V_s therein through said signal line 8; a display signal voltage generator 16 for generating said display signal voltage V_s ; an illuminating state controller for controlling a selection of an illuminating state or a non-illuminating state for each of said plurality of pixels at a time; and a constant voltage supply for supplying a constant voltage V_{il} to each of said plurality of pixels through said signal line 8 when said illuminating state is selected for said selected pixel. One end of said electro-luminescent element 1 provided in each said pixel 10 is connected to a common power supply while the other end of said electro-luminescent element 1 is selectively connected to a first source/drain electrode of an electro-luminescent element driving transistor 2 through a first switch 7, said transistor 2 has a threshold voltage V_{th} , a second source/drain electrode of said electro-luminescent element driving transistor 2 is connected to a power supply line 9 applied with a prescribed voltage (from a power input line 13 in Fig. 1), and the gate of said electro-luminescent element driving transistor 2 is connected to the signal line 8 through a capacitance 4 and selectively connected to the first source/drain electrode of said electro-luminescent element driving transistor 2 through a second switch 6 (claim 2; Fig. 2). When said illuminating state is selected (during a “illuminating period”, 2nd half of the frame in Fig. 3), the first switch 7 is fixed as ON, the second switch 6 is fixed as OFF, and the constant voltage V_{il} lower than display signal voltage V_s is applied to the signal line 8 (Fig. 1; *“the signal line switch 17 switches the signal line 8 between the signal voltage generation circuit 16 and the constant voltage input line 14”* p. 10, lines 1-4) such that a voltage that is lower than said prescribed voltage (e.g., by $(V_s - V_{il} + |V_{th}|)$); claim 29) appears at the gate of said transistor 2 (Fig. 3; p. 13, lines 19-25; p. 14, lines 5-11).

Applicants contend that none of the cited prior art references teaches or suggests “supplying a constant voltage V_{il} to each of said plurality of pixels through said signal line 8 when said illuminating state is selected for said selected pixel (claim 1, lines 10-12),” while “a second source/drain electrode of said electro-luminescent element driving transistor 2 is connected to a power supply line 9 applied with a prescribed voltage (claim 1, lines 18-20),

and the gate of said electro-luminescent element driving transistor 2 is connected to the signal line 8 through a capacitance 42 (claim 1, lines 21-22)” as according to the invention.

As recited in claim 13, one end of the signal line 8 is connected to the display signal voltage generator 16 and a constant voltage generator (“*constant voltage supplying means for supplying a constant voltage to each pixel through a signal line*” p. 5, lines 24-25; “*the signal line switch 17 switches the signal line 8 between the signal voltage generation circuit 16 and the constant voltage input line 14*” p. 10, lines 1-4) through a third switch 17 (Fig. 1).

In claim 30, when said illuminating state is selected, said electro-luminescent element is driven to by a voltage of ($V_s - V_{il}$) to illuminate. In claim 31, the constant voltage V_{il} applied to the signal line is the lowest level of said display signal voltage V_s (Figs. 3-4; Fig. 4 shows the details of the writing period of Fig. 3, to connect the two figures, V_{il} = lowest level of V_s).

As admitted by the Examiner (p. 4, 3rd paragraph of the outstanding Office Action), Akimoto does not disclose supplying a constant voltage to each pixel during the illuminating state or that the constant voltage is lower than the common supply voltage. In particular, Akimoto does not disclose supplying a constant voltage via a signal line to each pixel during the illuminating state, and the signal line is connected to the terminal of gate of the electro-luminescent element driving transistor.

Stewart was relied upon by the Examiner (p. 4, 4th paragraph of the outstanding Office Action) to provide such teachings. Contrary to the Examiner’s assertion that D2 (Fig. 4) is a signal line grounded by the voltage drop in the illuminated period, D2 of the first embodiment depicted in Figs. 1-4 is equivalent to the power line in the present invention, since D2 is connected to a source/drain of T2 (through TI) driving OLED 210 in Fig. 2 as the power line recited in claim 1, lines 18-20. It is natural that the power line D2 is under a constant voltage. The other embodiments of Stewart, such as the one shown in Fig. 6, share the same deficiencies as those of the first embodiment.

As such, Stewart only supplies a constant voltage to a power supply line D2 connected to a source/drain of the OLED 210 in the illuminated period, but not to a signal line D1 connected to the gate of the OLED 210 in the illuminated period as in the present invention.

Applicants contend that neither Akimoto, Stewart, nor their combination teaches or suggests each and every feature of the present invention as disclosed in independent claim 1. As such, the present invention as now claimed is distinguishable and thereby allowable over

the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

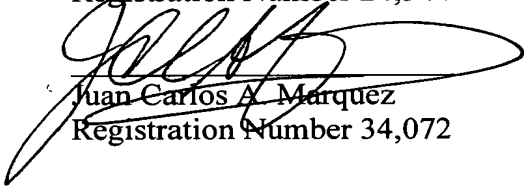
Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

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